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STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER	
POPHAM, JEFFREY D	
ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/004,458	FUNG ET AL.	
	Examiner	Art Unit	
	JEFFREY D. POPHAM	2137	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 December 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-18 and 20-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-18 and 20-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 September 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Remarks

Claims 1-4, 6-18, and 20-26 are pending.

Response to Arguments

1. Applicant's arguments filed 12/17/2007 have been fully considered but they are not persuasive.

Applicant argues that Blaner does not teach processing first data in a first processing engine and processing second data in a second processing engine. Blaner, column 9, lines 4-9 show that a program "checks the interrupt status registers 25 to determine whether a status bit, indicating an interrupt, is set for any of the functional unites (including the E unit). If a status bit is set in one or more registers, the program gets the instruction number from each functional unit which produced the interrupt." This clearly shows a plurality of processing engines (functional units) that can produce interrupts with regard to instructions.

Applicant also argues that Blaner fails to teach enabling a first interrupt indicator in a younger control record when processing of second data is complete. Regarding this argument, Applicant points to paragraph 37 of the present specification as teaching that an interrupt indicator "causes a core to issue an interrupt." This appears, however, to be an example of what an interrupt generator may be. The entire sentence referred to reads "An interrupt generator may be an interrupt indicator that causes a core to issue an interrupt." Therefore, this interrupt generator may be a certain kind of interrupt indicator that causes a core to issue an interrupt; however, an interrupt indicator is not

so limited. Additionally, Blaner, column 6, lines 32-44 explicitly teaches that, even when a younger instruction completes processing first (and an associated interrupt has occurred earlier than an interrupt associated with the older instruction), the interrupt for the older instruction will be reported before the interrupt for the younger instruction.

Applicant argues that Nakaya in view of Yamaura does not teach moving a first interrupt indicator associated with a younger control record onto a second interrupt indicator associated with an older control record if processing of the second data completes before processing of the first data. As basis for this argument, Applicant argues that "the Examiner refers to FIG. 7 of Nakaya and equates, for example, instructions U2 through U6, which are executed in parallel on separate processors P2-P6, as being younger instructions compared to instruction U1, executed on processor P1 (U1 being the older instruction)" and that "the older instruction U1 can never finish **after** the parallel execution of younger instructions U2 through U6."

As described in the office action mailed on 7/17/2007, Figure 7 of Nakaya shows a sequence of instructions, from U1 to U13. Each instruction in this sequence is older than all instructions that are after it, and younger than all instructions that are before it, numerically. Therefore, instruction U1 is older than all other instructions, U2 is younger than U1 and older than U3-U13, U3 is younger than both U1 and U2, and older than U4-U13, and so on. Instruction U3 is **not** equally old as instruction U2, as Applicant appears to contend. U2 is still an older instruction that U3, even if they are processed in parallel. Indeed, if 2 pieces of data must explicitly be processed in sequence (processing of the first data must complete before processing of the second data can

begin), then processing of the second data can never be complete before processing of the first data. From this, it should be clearly seen that Nakaya teaches the claimed moving of a first interrupt indicator associated with a younger control record onto a second interrupt indicator associated with the older control record if processing of the second data completes before processing of the first data.

Applicant goes on to argue that claim does not contend delaying the issuance of an interrupt until all processing engines have completed their respective tasks, but that claim 1 results in delaying the issuance of an interrupt **only** if processing of the second, younger data completes before processing of the first, older data. While it may be true that Nakaya has the additional functionality of delaying the issuance of an interrupt until all processing engines have completed their tasks, this is not forbidden by claim 1. Claim 1 does not describe what occurs if processing of the first data associated with the older control record completes first. There is nothing in claim 1 that limits any delaying of an interrupt to occurring **only** when processing of the second data completes first, so whether Nakaya teaches additional delay features is insignificant regarding the claims of the current application.

Claim Objections

2. Claims 3 and 6 are objected to because of the following informalities: Claims 3 and 6 each used to refer to "the second interrupt indicator" twice, and now refer to "the first interrupt indicator" once and "the second interrupt indicator" once. Claim 6, for example, refers to "the second interrupt indicator associated with the younger control

record," however the second interrupt indicator is associated with the older control record (as stated in claim 1). For purposes of prior art rejection, all interrupt indicators within claims 3 and 6 have been construed as the “first interrupt indicator" so as to provide antecedent basis and to correlate to previous instances of such claims (both interrupt indicators stated in each claim referring to the same interrupt indicator).

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 3, 4, 8, and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Blaner (U.S. Patent 5,003,462).

Regarding Claim 1,

Blaner discloses a method for processing data using a plurality of processing engines, the method comprising:

Processing first data associated with an older control record in a first processing engine (Column 5, line 41 to Column 6, line 44; and Column 8, line 62 to Column 9, line 30);

Processing second data associated with a younger control record in a second processing engine (Column 5, line 41 to Column 6, line 44; and Column 8, line 62 to Column 9, line 30);

Enabling a first interrupt indicator in the younger control record when the processing of the second data is completed (Column 5, line 41 to Column 6, line 44; and Column 8, line 62 to Column 9, line 30); and

Moving the first interrupt indicator associated with the younger control record onto a second interrupt indicator associated with the older control record if processing of the second data completes before processing of the first data (Column 5, line 41 to Column 6, line 44; and Column 8, line 62 to Column 9, line 30).

Regarding Claim 3,

Blaner discloses that moving the first interrupt indicator comprises determining that the first interrupt indicator is enabled (Column 5, line 41 to Column 6, line 44; and Column 8, line 62 to Column 9, line 30).

Regarding Claim 4,

Blaner discloses that moving the first interrupt indicator comprises delaying the generation of an interrupt associated with the younger control record (Column 5, line 41 to Column 6, line 44; and Column 8, line 62 to Column 9, line 30).

Regarding Claim 8,

Blaner discloses that the older control record comprises a reference to data (Column 5, line 41 to Column 6, line 44; and Column 8, line 62 to Column 9, line 30).

Regarding Claim 9,

Blaner discloses that the older control record comprises a reference to an operation to be performed on data (Column 5, line 41 to Column 6, line 44; and Column 8, line 62 to Column 9, line 30).

4. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Blaner in view of Pierson (Pierson et al., "Context-Agile Encryption for High Speed Communication Networks", Computer Communications Review, Association for Computing Machinery, Vol. 29, No. 1, January 1999, pp. 35-49).

Blaner does not explicitly disclose that the first processing engine is a public key engine.

Pierson, however, discloses that the first processing engine is a public key engine (Pages 46-48, Section 5.2). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to incorporate the cryptographic system of Pierson into the interrupt sequencing and reporting system of Blaner in order to allow the system to perform encryption and authentication quickly and easily, encrypting multiple communications (with different keys, algorithms, etc.) at a time without the normal delay required for context switching.

5. Claims 6, 7, and 10-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Blaner in view of Yamaura (U.S. Patent 6,175,890).

Regarding Claim 6,

Blaner may not explicitly disclose that moving the second interrupt indicator comprises setting the second interrupt indicator associated with the younger control record to disabled.

Yamaura, however, discloses that moving the first interrupt indicator comprises setting the first interrupt indicator associated with the younger control record to disabled (Column 1, lines 12-30; and Column 4, line 59 to Column 5, line 10). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to incorporate the interrupt masking system of Yamaura into the interrupt sequencing and reporting system of Blaner in order to efficiently save and restore data to be communicated to an external processor.

Regarding Claim 7,

Blaner as modified by Yamaura discloses the method of claim 6, in addition, Blaner discloses that moving the first interrupt indicator further comprises setting the second interrupt indicator associated with the older control record to enabled (Column 5, line 41 to Column 6, line 44; and Column 8, line 62 to Column 9, line 30).

Regarding Claim 10,

Blaner may not explicitly disclose writing processed data to memory associated with a host.

Yamaura, however, discloses writing processed data to memory associated with a host (Column 4, line 59 to Column 5, line 49). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to incorporate the interrupt masking system of Yamaura into the interrupt sequencing and reporting system of Blaner in order to efficiently save and restore data to be communicated to an external processor.

Regarding Claim 11,

Blaner as modified by Yamaura discloses the method of claim 10, in addition, Blaner discloses that the processing engines are coupled to an interrupt handler (Column 5, line 41 to Column 6, line 44; and Column 8, line 62 to Column 9, line 30) and Yamaura discloses that the external processor is coupled to the interrupt handler (Figure 1).

Regarding Claim 12,

Blaner as modified by Yamaura discloses the method of claim 11, in addition, Blaner discloses that the processing engines are coupled to a scheduler (Column 5, line 41 to Column 6, line 44; and Column 8, line 62 to Column 9, line 30) and Yamaura discloses that the external processor is coupled to the scheduler (Figure 1).

Regarding Claim 13,

Blaner as modified by Yamaura discloses the method of claim 12, in addition, Blaner discloses generating an interrupt when processing of the older control record has been completed (Column 5, line 41 to Column 6, line 44; and Column 8, line 62 to Column 9, line 30).

Regarding Claim 14,

Blaner as modified by Yamaura discloses the method of claim 13, in addition, Yamaura discloses that the external processor reads the processed data when the interrupt is generated (Column 4, line 59 to Column 5, line 49).

6. Claims 1, 3, 4, and 6-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakaya (U.S. Patent 5,978,830) in view of Yamaura.

Regarding Claim 1,

Nakaya discloses a method for processing data using a plurality of processing engines, the method comprising:

Processing first data associated with an older control record in a first processing engine (Column 12, lines 10-62; and Column 25, line 40 to Column 26, line 12);

Processing second data associated with a younger control record in a second processing engine (Column 12, lines 10-62; and Column 25, line 40 to Column 26, line 12);

Issuing a first interrupt indicator (termination notice) when the processing of the second data is completed (Column 12, lines 10-62; and Column 25, line 40 to Column 26, line 12); and

Moving the first interrupt indicator associated with the younger control record onto a second interrupt indicator associated with the older control record if processing of the second data completes before processing of the first data (Column 12, lines 10-62; and Column 25, line 40 to Column 26, line 12);

But does not disclose the enablement of a first interrupt indicator in the younger control record.

Yamaura, however, discloses enabling a first interrupt indicator associated with the younger control record (Column 1, lines 12-30; and Column 4, line 59 to Column 5, line 10).

Where the interrupt indicator is placed, whether it be in a register devoted to interrupt indicators and their associations to control records or within the control record itself, is of no significance to this method, since placing the interrupt indicator within the control record does not provide an advantage over using a register to store the indicator.

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to incorporate the interrupt handling method of Yamaura into the parallel job schedule system of Nakaya in order to efficiently restore data to be communicated to an external processor.

Regarding Claim 3,

Nakaya as modified by Yamaura discloses the method of claim 1, in addition Yamaura discloses that moving the first interrupt indicator comprises determining that the first interrupt indicator is enabled (Column 1, lines 12-30; and Column 4, line 59 to Column 5, line 10).

Throughout this action, when the moving (or collapsing) of interrupt indicators is cited as being in Yamaura, it is to be understood that Yamaura teaches the foundations of how it is done, via the enabling and disabling of interrupt indicators within the interrupt controller, while the portion of Nakaya cited above discloses the moving of interrupt indicators (not issuing an interrupt until termination notices from all of the processors are issued).

Regarding Claim 4,

Nakaya as modified by Yamaura discloses the method of claim 1, in addition, Nakaya discloses that moving the first interrupt indicator comprises delaying the generation of an interrupt associated with the younger control record (Column 25, lines 40-63). The termination notices are issued at all of the processors before any one of the processors can generate the interrupt.

Regarding Claim 6,

Nakaya as modified by Yamaura discloses the method of claim 4, in addition, Yamaura discloses that moving the first interrupt indicator

comprises setting the first interrupt indicator associated with the younger control record to disabled (Column 1, lines 12-30; and Column 4, line 59 to Column 5, line 10).

Regarding Claim 7,

Nakaya as modified by Yamaura discloses the method of claim 6, in addition, Yamaura discloses that moving the first interrupt indicator further comprises setting the second interrupt indicator associated with the older control record to enabled (Column 1, lines 12-30; and Column 4, line 59 to Column 5, line 10).

Regarding Claim 8,

Nakaya as modified by Yamaura discloses the method of claim 1, in addition, Nakaya discloses that the older control record comprises a reference to data (Column 12, lines 13-29).

Regarding Claim 9,

Nakaya as modified by Yamaura discloses the method of claim 8, in addition, Nakaya discloses that the older control record comprises a reference to an operation to be performed on data (Column 12, lines 13-29).

Regarding Claim 10,

Nakaya as modified by Yamaura discloses the method of claim 1, in addition, Yamaura discloses writing processed data to memory associated with a host (Column 4, line 59 to Column 5, line 49).

Regarding Claim 11,

Nakaya as modified by Yamaura discloses the method of claim 10, in addition, Nakaya discloses that the processing engines are coupled to the interrupt controller (Figure 1); and Yamaura discloses that the external processor is coupled to the interrupt controller (Figure 1).

Regarding Claim 12,

Nakaya as modified by Yamaura discloses the method of claim 11, in addition, Nakaya discloses that the interrupt controller is coupled to the processing engines through a scheduler (synchronizer) (Figure 1).

Regarding Claim 13,

Nakaya as modified by Yamaura discloses the method of claim 12, in addition, Nakaya discloses generating an interrupt when processing of the older control record has been completed (Column 25, line 40 to Column 26, line 12).

Regarding Claim 14,

Nakaya as modified by Yamaura discloses the method of claim 13, in addition, Yamaura discloses that the external processor reads the processed data when the interrupt is generated (Column 4, line 59 to Column 5, line 49).

7. Claims 2, 15-18, and 20-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakaya in view of Yamaura, further in view of Pierson.

Regarding Claim 2,

Nakaya in view of Yamaura does not disclose that the first processing engine is a public key engine.

Pierson, however, discloses that the first processing engine is a public key engine (Pages 46-48, Section 5.2). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to incorporate the cryptographic system of Pierson into the parallel job scheduling system of Nakaya as modified by Yamaura in order to allow the system to perform encryption and authentication quickly and easily, encrypting multiple communications (with different keys, algorithms, etc.) at a time without the normal delay required for context switching.

Regarding Claim 15,

Nakaya discloses an apparatus, comprising:

A first processing engine configured to receive a first control record (Column 12, lines 10-62; and Column 25, line 40 to Column 26, line 12);

A second processing engine configured to receive a second control record (Column 12, lines 10-62; and Column 25, line 40 to Column 26, line 12);

A history buffer (interrupt controller/synchronizer) containing information associated with the first and second control records including a first interrupt indicator associated with the first control record and a

second interrupt indicator associated with the second control record (Column 12, lines 10-62; and Column 25, line 40 to Column 26, line 12),

Wherein the history buffer is configured to move the first interrupt indicator associated with the first control record onto a second interrupt indicator associated with the second control record if processing of the first control record completes before processing of the second control record (Column 12, lines 10-62; and Column 25, line 40 to Column 26, line 12);

But does not disclose that the apparatus is a cryptography accelerator; or an interface coupled to an external processor and memory associated with the external processor.

Yamaura, however, discloses an interface coupled to an external processor and memory associated with the external processor; the interface being coupled to the processing engines as well (Column 1, lines 12-30; Column 4, line 59 to Column 5, line 10; and Figure 1). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to incorporate the interrupt handling method of Yamaura into the parallel job schedule system of Nakaya in order to efficiently restore data to be communicated to an external processor.

Pierson discloses that the apparatus is a cryptography accelerator (Pages 46-48, Section 5.2). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to incorporate the

cryptographic system of Pierson into the parallel job scheduling system of Nakaya as modified by Yamaura in order to allow the system to perform encryption and authentication quickly and easily, encrypting multiple communications (with different keys, algorithms, etc.) at a time without the normal delay required for context switching.

Regarding Claim 16,

Nakaya as modified by Yamaura and Pierson discloses the apparatus of claim 15, in addition, Pierson discloses that the first processing engine is a public key engine (Pages 46-48, Section 5.2).

Regarding Claim 17,

Nakaya as modified by Yamaura and Pierson discloses the apparatus of claim 15, in addition, Nakaya discloses that the history buffer is configured to collapse the first interrupt indicator associated with the first control record onto the second interrupt indicator associated with the second control record (Column 12, lines 10-62; and Column 25, line 40 to Column 26, line 12), and Yamaura discloses that this is performed when the first interrupt indicator is enabled (Column 1, lines 12-30; and Column 4, line 59 to Column 5, line 10).

Regarding Claim 18,

Nakaya as modified by Yamaura and Pierson discloses the apparatus of claim 17, in addition, Nakaya discloses that collapsing the first interrupt indicator associated with the first control record onto the

second control record further comprises delaying the generation of an interrupt associated with the first control record (Column 12, lines 10-62; and Column 25, line 40 to Column 26, line 12).

Regarding Claim 20,

Nakaya as modified by Yamaura and Pierson discloses the apparatus of claim 18, in addition, Yamaura discloses that collapsing the first interrupt indicator associated with the first control record onto the second control record further comprises setting the first interrupt indicator associated with the first control record to disabled (Column 1, lines 12-30; and Column 4, line 59 to Column 5, line 10).

Regarding Claim 21,

Nakaya as modified by Yamaura and Pierson discloses the apparatus of claim 20, in addition, Yamaura discloses that collapsing the first interrupt indicator associated with the first control record onto the second control record further comprises setting the second interrupt indicator associated with the second control record to enabled (Column 1, lines 12-30; and Column 4, line 59 to Column 5, line 10).

Regarding Claim 22,

Nakaya as modified by Yamaura and Pierson discloses the apparatus of claim 15, in addition, Nakaya discloses that the second control record comprises a reference to data (Column 12, lines 13-29).

Regarding Claim 23,

Nakaya as modified by Yamaura and Pierson discloses the apparatus of claim 22, in addition, Nakaya discloses that the second control record comprises a reference to an operation to be performed on data (Column 12, lines 13-29).

Regarding Claim 24,

Nakaya as modified by Yamaura and Pierson discloses the apparatus of claim 23, in addition, Nakaya discloses that the external processor is coupled to the processing engines through a scheduler (synchronizer) (Figure 1).

Regarding Claim 25,

Nakaya as modified by Yamaura and Pierson discloses the apparatus of claim 24, in addition, Nakaya discloses that an interrupt is generated when processing of the second control record has been completed (Column 25, line 40 to Column 26, line 12).

Regarding Claim 26,

Nakaya as modified by Yamaura and Pierson discloses the apparatus of claim 25, in addition, Yamaura discloses that the external processor reads the processed data when the interrupt is generated (Column 4, line 59 to Column 5, line 49).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JEFFREY D. POPHAM whose telephone number is (571)272-7215. The examiner can normally be reached on M-F 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Emmanuel Moise can be reached on (571)272-3865. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jeffrey D Popham
Examiner
Art Unit 2137

/Jeffrey D Popham/
Examiner, Art Unit 2137

/Emmanuel L. Moise/
Supervisory Patent Examiner, Art Unit 2137